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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/749,792
Filing Date: December 28, 2000
Appellant(s): CAI, ZHONG-NING (GEORGE)

William E. Curry
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 24, 2005 appealing from the Office action mailed March 21, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal: None.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Patent 5940785	Georgiou et al.	8-1999
US Patent 5233314	McDermott et al.	8-1993
US Patent 6192479	Ko	2-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1-4, 6-9, 11-17

2. Claims 1-4, 6-9, 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou et al, U.S. Patent 5940785, hereinafter referred to as Georgiou, in view of McDermott et al., U.S. Patent 5233314, hereinafter referred to as McDermott.

3. In re claim 1, Georgiou disclose an apparatus for dynamic power control of a processor based on a thermal condition [abstract], comprising:

- A sensor to measure a thermal characteristic of a processor with a clock frequency [119, fig.1].
- A circuit to reduce the clock frequency of the processor [col.3, ll.60–64, col.4, ll.35–37, 48–50] responsive to the measured thermal characteristic satisfying a predetermined threshold [col.4, ll.26–33], the circuit including an input [270; rate of temperature change] to determine a temperature-related frequency reduction [col.4, ll.26-50].

4. Georgiou did not disclose expressly a performance demanding level input to determine a ***rate*** of the frequency reduction.

5. McDermott taught an apparatus [fig.1] for dynamic power control of a processor [cpu 4] [col.1, l.13 – col.3, l.23] comprising:

- A circuit [clock generator 10] to reduce the clock frequency of the processor, the circuit including a performance demanding level input [lvl1, 2] to determine a rate of the frequency reduction [col.4, l.66 – col.5, l.24; col.6, ll.51-64; col.8, l.45 – col.9, l.13].

6. It would have been obvious to one of ordinary skill in the art, having the teachings of Georgiou and McDermott before him at the time the invention was made, to modify ***the circuit that includes an input to determine a temperature-related frequency reduction*** as taught by Georgiou to include the teachings regarding ***controlling frequency reductions via a rate*** as taught by McDermott, in order to obtain the apparatus for dynamic power control of a processor based on a thermal condition, comprising a circuit to reduce the clock frequency of the processor responsive to the measured thermal characteristic satisfying a pre-determined threshold, ***the circuit including a performance demanding level input to determine a rate of the temperature-related frequency reduction***. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better control frequency changes [McDermott: col.2, l.65 – col.3, l.23].

7. As per claim 2, Georgiou taught the thermal characteristic which includes temperature and rate of temperature change [col. 4, lines 26 – 33].

8. As per claim 3, Georgiou taught a frequency generator and a logic circuit [fig. 4, col. 8, line 42 – 66].

9. As per claim 4, Georgiou reduces the clock frequency by less than fifty percent [col. 8, lines 48 – 49].

10. As per claim 6, Georgiou would slow down the processor when it runs too hot thereby allowing the processor, inherently, to run at a higher operating temperature.

11. As per claims 7 – 9 and 11, Georgiou and McDermott taught each and every limitation as discussed above in reference to claims 1-4 and 6. Therefore, Georgiou and McDermott taught the method in operating the apparatus.

12. In re claim 12, Georgiou and McDermott disclose each and every limitation as discussed above in reference to claim 1. Georgiou further taught the steps of:

- Entering a first state [normal operating state with normal clock frequency] from a second state [overheat state] in response to a measured thermal characteristic of a processor with a clock frequency failing to satisfy a first predetermined threshold [threshold temperature 230 which indicates the processor is overheating][1] ;
- Remaining in the first state in response to a measured thermal characteristic of the processor failing to satisfy the first pre-determined threshold [the processor remain in the normal operating state when its temperature fails to rise above the threshold temperature]; and
- Entering the second state from the first state in response to a measured thermal characteristic of the processor satisfying the first predetermined threshold, and in the second state, performing frequency reduction [the processor enters the

[1] After the processor enters into a overheating state, the processor's clock frequency will be reduced until the processor is cooling off. Thereafter, the processor returns to its normal operating state, col. 9, lines 22 - 25.

overheating state when the heat sensor indicates the temperature is above the threshold temperature and reduces clock frequency to reduce temperature].

13. As per claims 13 – 17, Georgiou taught the usage of temperature and rate of temperature change of the predetermined thresholds [col.4, ll.30–34].

Re Claims 5 and 10

14. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Georgiou and McDermott as applied to claims 1 and 7 above, and further in view of Ko, U.S. Patent 6192479.

15. Georgious and McDermott disclose each and every limitation of the claim as discussed above in reference to claims 1 and 7. Georgiou and McDermott did not discuss the details of reducing the clock frequency.

16. Ko taught an invention for power management of a processing device, the invention comprising of a circuit for reducing the clock frequency by removing a pre-determined number of transitions from a signal producing the clock frequency [column 5, lines 53-58].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Georgiou, McDermott, and Ko before him at the time the invention was made, to include the teachings of Ko with the apparatus disclosed by Georgiou and McDermott as the way of reducing the clock frequency taught by Ko is a well known way suitable for reducing the clock frequency in the apparatus of Georgiou and McDermott. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce the clock frequency and better control power conservation [Ko: col.2, ll.10-35].

Re Claims 18-20

18. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ko in view of Georgiou and McDermott.

19. In re claim 18, Ko discloses a processor [data processing device 21] comprising:

- Thermal sensing logic [circuit 49] to output an enabling signal taking on values responsive to whether a temperature signal meets or do not meet predetermined temperature threshold [Tok] [col.8, ll.48-53].
- Performance demanding level logic [clock arbiter 51] to output a signal [down] taking on values that permit temperature-related frequency reduction [col.6, l.32 – col.7, l.5; temperature overheat signal induces clock arbiter to issue down signal to reduce frequency].
- Frequency reduction logic coupled to the performance demanding level logic and the thermal sensing logic, to perform frequency reduction based on the values generated by the thermal sensing logic and the performance demanding level logic [col.4, ll.49-60].

20. Ko did not discuss values representing a rate of temperature change or a rate of frequency reduction.

21. Regarding the rate of temperature change, Georgiou discloses a thermal sensing logic [119, 130] to output function signals taking on values representing a function of a temperature [relative to a prior sample] and a rate of temperature change [col.4, ll.17-50; col.7, ll.12-50].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Ko and Georgiou before him at the time the invention was made, to modify the processor taught by Ko to include the thermal sensing logic outputs taught by Georgiou, in order to obtain the

processor comprising thermal sensing logic to output function signals taking on values representing a function of a temperature and a rate of temperature change, and an enabling signal taking on values responsive to whether the function signals meets or do not meet predetermined temperature and rate of temperature change thresholds. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for better clock control for power conservation [Ko: col.2, ll.10-35; Georgiou: col.3, ll.17-46].

23. Regarding the rate of frequency reduction, McDermott discloses a performance demanding logic [14] to output a signal [lvl1, 2] taking on values [high, low] that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second [col.4, l.66 – col.5, l.24; col.6, ll.51-64; col.8, l.45 – col.9, l.13].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Ko and McDermott before him at the time the invention was made, to modify the processor taught by Ko to include the performance demanding logic output taught by McDermott, in order to obtain the processor comprising a performance demanding logic to output a signal taking on values that respectively permit a first rate of frequency reduction and a second rate of frequency reduction, the first rate of frequency reduction being higher than the second. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to better control frequency changes [McDermott: col.2, l.65 – col.3, l.23].

25. As to claim 19, Georgiou discloses each and every limitation as discussed above in reference to claims 12-17.

26. As to claim 20, Ko discloses the processor wherein values output by the performance demanding level logic are responsive to a processor application [col.6, l.32 – col.7, l.5; down signal are responsive to functional unit activity status signal].

(10) Response to Argument

A. Claims 1-4, 6-9 and 11-17 are allowable over Georgiou et al. and McDermott [et al.].

Appellant's arguments with respect to part A have been fully considered but they are not persuasive as detailed in the following.

Appellant alleges Georgiou and McDermott "do not suggest a performance demanding level input to determine a rate of temperature-related frequency reduction". Specifically, Appellant has argued that ***McDermott*** fails to teach the performance demanding level input involved in frequency reduction ***based on temperature***. Examiner agrees *but* submits that the rejection was based on a *combination* of:

- **Georgiou,** the base reference, which teaches a ***general input*** [270] involved in frequency reduction ***based on temperature*** [col.4, ll.26-50]; and
- **McDermott** which teaches the concept of a ***performance demanding level input*** [LVL1, LVL2] involved in frequency reduction in general, with no explicit exclusion of any particular systems [i.e., McDermott's teachings would be applicable to any systems requiring frequency reduction, including the system based on temperature as taught by Georgiou].

Appellant is reminded that the test for obviousness is what would the references taken together suggest to one of ordinary skill in the art, not whether or not the elements of the secondary reference can be bodily incorporated into the primary reference. Georgiou and McDermott taken

together clearly suggest "a performance demanding level input to determine a rate of temperature related frequency reduction". One of ordinary skill in the art would be motivated by their combine teachings to implement ***the performance demanding level input involved in frequency reduction based on temperature*** in order to have better control of frequency changes via a performance demanding level input [McDermott: col.2, l.65 – col.3, l.23] for systems such as Georgiou's that is involved in frequency reduction based on temperature changes.

Appellant alleges that "McDermott clearly relate only to the synchronization of a PLL... at most the combination of Georgiou with McDermott yields Georgious's device plus an improve PLL". Firstly, Examiner notes Appellant's concession that McDermott does teach the synchronization of a PLL and submits that better control of frequency changes in any system [i.e., including a system involved in frequency reduction based on temperature changes as taught by Georgiou] requires an effective synchronization scheme in order to function properly. Secondly, Examiner notes Appellant's concession that the combination of Georgiou and McDermott would indeed yield an improved Georgiou's device based on an improved PLL as taught by McDermott. Examiner agrees that a PLL with a predetermined demanding level input to better control frequency reduction based on temperature changes is an improvement and provides proper motivation for the combination.

Appellant alleges there is "no credible motivation for the modification to Georgiou ... portion of McDermott cited ... do not motivate modification of a thermal throttling system for processors... rather, they motivate improvements to a PLL". Examiner strongly disagrees and submits the following. As indicated by Appellant on pages 8-9 of the appeal brief, McDermott "provide[s] a fully integrated charge pump PLL having a fast response time to input frequency

changes as well as highly stable behavior..." Examiner submits that at least the highly stable behavior in frequency changes is desirable in any system, including that of a thermal throttling system taught by Georgiou. If the system of Georgiou initiates a frequency reduction based on temperature change without a highly stable behavior, the subsequent processing based on the transitioned frequency would experience myriads of problems such as race conditions. Thus, the improved PLL of McDermott would enable the system of Georgiou to reduce frequency based on temperature at least in a highly stable behavior to avoid the problems of race conditions.

Appellant alleges McDermott "fails [*In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992)] test... McDermott is concerned with synchronization of a PLL, while the rejected claims relate to temperature related frequency reduction". As indicated by appellant, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. In this case, Examiner submits that McDermott is concerned with *frequency control* [col.1, ll.8-10], which is pertinent to temperature related *frequency reduction*. Furthermore, Examiner submits that PLLs are commonly used in frequency controls such as throttling or frequency reduction, including Appellant's claimed apparatus that also employs a PLL [item 310] in the frequency control process.

B. Claims 5 and 10 are allowable over Georgiou and McDermott in view of Ko.

Appellant's arguments with respect to part B have been fully considered but they are not persuasive as detailed in the following.

Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

C. Claims 18-20 are allowable over Ko in view of Georgiou and McDermott.

Appellant's arguments with respect to part C have been fully considered but they are not persuasive as detailed in the following.

Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Tse Chen

December 12, 2005

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